WHAT IS CLAIMED IS:

1. An adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising:

a bypass input (*bypass*); and

a logic circuit, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the logic circuit configured to hold at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

2. The adder of claim 1, wherein the logic circuit further generates the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

3. The adder of claim 1, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the logic circuit further holds the carry input (*C)* according to the bypass input (*bypass*).

4. The adder of claim 1, wherein the logic circuit further generates the carry output *(CARRY)* without computing a new output according to the bypass signal (*bypass*).

5. The adder of claim 1, wherein the logic circuit comprises a transmission gate adder.

6. The adder of claim 5, wherein the transmission gate adder comprises:

a first multiplexer having a first multiplexer first input communicatively coupled to the first input *(A)*, a first multiplexer second input, and a first multiplexer control input;

a second multiplexer having a second multiplexer first input communicatively coupled to the second input *(B)*, a second multiplexer second input, and a second multiplexer control input;

a first logic module having a first logic module first input, a first logic module second input, and a first logic module output, the first logic module output having an EXCLUSIVE OR relationship between the first logic module first input and the first logic module second input; and

wherein the first logic module input is communicatively coupled to the first input *(A)*, the logic module second input is communicatively coupled to the second input *(B)*, and the first logic module output is communicatively coupled to the first multiplexer control input and the second multiplexer control input.

7. The adder of claim 6, wherein the first logic module is an EXCLUSIVE OR gate.

8. The adder of claim 7, further comprising:

a first inverter communicatively coupled between the first input *(A)* and the first multiplexer first input; and

a second inverter communicatively coupled between the second input *(B)* and second multiplexer first input.

9. The adder of claim 1, wherein the logic circuit is configured to hold the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

10490 - 08/659560

10. The adder of claim 9, wherein the logic circuit comprises a transmission gate adder.

11. The adder of claim 10, wherein the transmission gate adder comprises:

a first multiplexer having a first multiplexer first input communicatively coupled to the first input *(A)*, a first multiplier second input, and a first multiplexer control input;

a second multiplexer having a second multiplexer first input communicatively coupled to the second input *(B)*, a second multiplier second input, and a second multiplexer control input;

a first logic module having a first logic module first input, a first logic module second input, and a first logic module output, the first logic module output having an EXCLUSIVE OR relationship between the first logic module first input and the first logic module second input; and

wherein the first logic module input is communicatively coupled to the first input *(A)*, the logic module second input is communicatively coupled to the second input *(B)*, and the first logic module output is communicatively coupled to the first multiplexer control input and the second multiplexer control input.

12. The adder of claim 6, wherein the logic circuit comprises:

a second logic module having a second logic module first input, a second logic module second input, and a second logic module output, the second logic module output having an EXCLUSIVE OR relationship between the second logic module first input and the second logic module second input; and

wherein the second logic module first input is communicatively coupled to the first logic module output.

13. The adder of claim 12, wherein the second logic module is an EXCLUSIVE OR gate.

14. A device for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising

a bypass input (*bypass*); and

a logic circuit, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the logic circuit configured to generate the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

15. The device of claim 14, wherein the logic circuit is further configured to hold at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

16. The device of claim 14, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the logic circuit further holds the carry input (*C*) according to the bypass input (*bypass*).

17. The device of claim 14, wherein the logic circuit further regenerates the carry output *(CARRY)* without computing a new output according to the bypass signal (*bypass*).

18. An adder for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising:

a bypass input (*bypass*); and

a holding means for holding at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*); and

wherein the holding means is communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the holding means configured to hold at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

19. The adder of claim 18, wherein the holding means further comprises means for generating the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

20. The adder of claim 18, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the holding means further holds the carry input (*C*) according to the bypass input (*bypass*).

21. The adder of claim 18, wherein the holding means further generates the carry output *(CARRY)* without computing a new output according to the bypass signal (*bypass*).

22. The adder of claim 21, wherein the holding means comprises a transmission gate adder.

23. The adder of claim 22, wherein the transmission gate adder comprises:

a first multiplexing means having a first multiplexing means first input communicatively coupled to the first input *(A)*, a first multiplexing means second input, and a first multiplexing means control input;

a second multiplexing means having a second multiplexing means first input communicatively coupled to the second input *(B)*, a second multiplexing means second input, and a second multiplexing means control input;

a first logic means having a first logic means first input, a first logic means second input, and a first logic means output, the first logic means output having an EXCLUSIVE OR relationship between the first logic means first input and the first logic means second input; and

wherein the first logic means input is communicatively coupled to the first input *(A)*, the first logic means second input is communicatively coupled to the second input *(B)*, and the first logic means output is communicatively coupled to the first multiplexing means control input and the second multiplexing means control input.

24. The adder of claim 23, further comprising:

a first inverting means communicatively coupled between the first input *(A)* and the first multiplexing means first input; and

a second inverter communicatively coupled between the second input *(B)* and second multiplexing means first input.

25. The adder of claim 18, wherein the holding means is configured to hold the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

26. The adder of claim 25, wherein the holding means comprises a transmission gate adder.

27. The adder of claim 26, wherein the transmission gate adder comprises:

a first multiplexing means having a first multiplexing means first input communicatively coupled to the first input *(A)*, a first multiplexing means second input, and a first multiplexing means control input;

a second multiplexing means having a second multiplexing means first input communicatively coupled to the second input *(B)*, a second multiplexing means second input, and a second multiplexing means control input;

a first logic means having a first logic means first input, a first logic means second input, and a first logic means output, the first logic means output having an EXCLUSIVE OR relationship between the first logic means first input and the first logic means second input; and

wherein the first logic means input is communicatively coupled to the first input *(A)*, the logic means second input is communicatively coupled to the second input *(B)*, and the first logic means output is communicatively coupled to the first multiplexing means control input and the second multiplexing means control input.

28. The adder of claim 27, wherein the logic means comprises:

a second logic means having a second logic means first input, a second logic means second input, and a second logic means output, the second logic means output having a relationship selected from a group comprising an EXCLUSIVE OR relationship and a multiplexing relationship between the second logic means first input and the second logic means second input; and

wherein the second logic means first input is communicatively coupled to the first logic means output.

09936978 - 062501

29. A device for adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising:

a bypass input (*bypass*); and

a generating means, communicatively coupled to the bypass input (*bypass*), the first input *(A)*, and the second input *(B)*, the generating means configured to generate the adder output *(S)* without computing a new adder output according to the bypass input (*bypass*).

30. The device of claim 29, wherein the generating means is further configured to hold at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

31. The device of claim 29, further comprising:

a carry input *(C)* and a carry output *(CARRY)*; and

wherein the generating means further holds the carry input (*C*)according to the bypass input (*bypass*).

32. The device of claim 29, wherein the generating means further generates the carry output *(CARRY)* without computing a new output according to the bypass signal (*bypass*).

33. A method of adding a signal at a first input *(A)* and a second input *(B)* to produce an adder output *(S)*, comprising the steps of:

accepting a bypass input (*bypass*); and

holding at least one of the first input *(A)* and the second input *(B)* according to the bypass input (*bypass*).

34. The method of claim 33, further comprising the step of generating the adder output without computing a new adder output according to the bypass input (*bypass*).

35. The method of claim 33, further comprising the step of:

holding a carry input *(C)* according to the bypass input (*bypass*).

36. The method of claim 33, further comprising the step of:

generating the carry output *(CARRY)* without computing a new output according to the bypass signal (*bypass*).

37. A logic circuit that maps one or more inputs $A, B, \cdots$ to produce one or more outputs $S1, S2, \cdots$ according to a mapping function, comprising:

a bypass input; and

a first logic circuit element communicatively coupled to the bypass input;

a second logic circuit element, communicatively coupled to at least one of the inputs $A, B, \cdots$ that conditionally holds one of the inputs $A, B, \cdots$ according to the bypass input.

38. The logic circuit of claim 37, wherein the mapping function is describable by a truth table.

39. The logic circuit of claim 38, wherein the logic circuit is an adder that adds the one or more inputs $A, B, \cdots$ to produce the one or more outputs $S1, S2, \cdots$.

40. The logic circuit of claim 37, wherein the logic circuit further generates at least one of the outputs $S1, S2, \cdots$ without computing a new output $S1, S2, \cdots$ according to the bypass input.

41. The logic circuit of claim 37, wherein the logic circuit holds more than one of the inputs $A, B, \cdots$ according to the bypass input.

42. The logic circuit of claim 37, wherein the logic circuit is an adder and the logic circuit further comprises:

a carry input and a carry output; and

wherein the logic circuit further holds the carry input according to the bypass input.

43. The logic circuit of claim 42, wherein the logic circuit further regenerates the carry input according to the bypass input.

44. The logic circuit of claim 37, wherein the second logic circuit element comprises at least one latch communicatively coupled to at least one of the inputs $A, B, \cdots$, wherein the latch includes a logical input, a clock input, and an output, and the latch presents the logical input to the output only in response to a signal at the clock input.

45. A method of mapping one or more inputs $A, B, \cdots$ to produce one or more outputs $S1, S2, \cdots$ according to a mapping function, comprising the steps of:

accepting a bypass input; and

conditionally holding one of the inputs $A, B, \cdots$ according to the bypass input.

46. The method of claim 45, further comprising the step of:

generating at least one of the outputs $S1, S2, \cdots$ without computing a new output $S1, S2, \cdots$ according to the bypass input.

47. The method of claim 46, further comprising the step of generating at least another of the outputs $S1, S2, \cdots$ without computing a new another output $S1, S2, \cdots$ according to the bypass input.

48. The method of claim 45, further comprising the step of:

holding at least a second one of the inputs $A, B, \cdots$ according to the bypass input.